REMARKS

The Applicant thanks the Examiner for the thorough examination of the application. No new matter is believed to be added to the application by this Amendment.

Status of the Claims

Claims 1-18 are pending in the application. The amendments to claims 1 and 11 find support in Figures 4 and 6 and at paragraphs 0053 and 0063 of the specification. Claims 17 and 18 find support 0054 and 0064 of the specification.

Rejection Under 35 U.S.C. §103(a) Over Uchino and Nakano (and Itakura)

Claims 1, 3-5, 7-9 and 11-16 are rejected under 35 U.S.C. §103(a) as being obvious over Uchino (U.S. Patent 6,040,816) in view of Nakano (U.S. Patent 6,529,181). The Examiner adds the teachings of Itakura (U.S. Patent 5,252,957) to reject claims 2, 6 and 10. Applicant traverses.

The Present Invention and its Advantages

The present invention pertains to a novel LCD device that reduces power consumption and increases display quality by minimizing EMI (electromagnetic interference). One of the many novel features of the claimed invention resides in that at least two data buses are connected between the timing controller and respective source drivers. The inventive LCD device also utilizes a synchronized data sampling technology and timing controller configuration that minimizes the

use of unnecessary voltage, thereby decreasing power consumption. In another aspect of the invention, the source driver separately samples the digital R/G/B data so that the power consumption is reduced. Another of the novel features of the invention includes having the number of data buses being in proportion to the number of clock signals output from the timing controller.

The present invention finds a typical embodiment in instantly amended claim 1, which sets forth:

> 1. (Currently Amended) An LCD device, comprising:
> a LCD panel;
> a plurality of source drivers applying data signals to the LCD panel;
> a plurality of gate drivers applying gate driving signals to the LCD panel;
> a timing controller outputting to the source drivers at least two clock signals having different phases, the timing controller separately outputting R/G/B data synchronized with each output signal to the source drivers; and
> at least two data buses transmitting the data separately output from the timing controller to the source drivers,
> wherein the at least two data buses are connected between the timing controller and the respective source drivers.

As shown in Figure 4, source drivers 43 apply data signals to the LCD panel 41, and the gate driver 45 applies gate-driving signals to the LCD panel 41. The timing controller 47 receives a data clock signal DCLK and R/G/B digital data, and outputs first and second clock signals CLK1 and CLK2 having different phases and various control signals to control the source and gate drivers 43 and 45. The timing controller 47 connects to each source driver by at least two data buses (see also Figure 6), where a first data bus DB1 transmits the digital data synchronized with the first clock signal CLK1 to each source driver 43, and a

second data bus DB2 transmits the digital data synchronized with the second clock signal CLK2 to each source driver 43.

The advantages of using at least two data buses is described at paragraph 0053 of the specification:

> [0053] The timing controller 47 synchronizes digital data received from the system and synchronized with two clock signals through two data buses, and then separately outputs the synchronized digital data to the source drivers. As a result, electricity used in outputting the data can be reduced.

The advantages offered by the separate outputting of the timing controller 47 and the separate sampling of the source drivers 43 is explained in paragraph 0054 of the specification:

> [0054] The timing controller 47 separately outputs the digital data, so that the source driver 43 separately samples the digital data. Therefore, electricity used in sampling the digital data in the source driver 43 can be reduced, thereby substantially reducing electricity for driving the whole circuit as compared to the related art.

The advantages of the relationship between the timing controller 47 and the source drivers 43 are also explained in paragraphs 0063 (which utilizes three data buses) and 0064 of the specification:

> [0063] That is, the timing controller 47 separately outputs digital data received from the system and synchronized with the three clock signals per the R/G/B digital data through the three data buses to each source driver, thereby reducing the electric power used in outputting the data.
>
> [0064] Also, the timing controller 47 separately outputs digital data according to the R/G/B digital data, so that the source driver 43 separately samples the digital data according to the R/G/B digital

data. Therefore, the electric power consumption for driving the whole circuit can be reduced.

Distinctions of the Invention over Uchino, Nakano and Itakura

Distinctions of the invention over the prior art have been place before the Examiner. For brevity, these distinctions are not repeated in full here.

Uchino pertains to an active matrix display device with phase-adjusted sampling pulses. Figure 1 of Uchino shows a horizontal scan circuit 20 having a shift register 20a. The scan circuit 20 scans video signals S1, S2, S3 . . . and outputs sampling pulse A1, A2, A3 . . . to logical circuits 70a, 70b, 70c . . . to disperse the sampling pulses B1, B2, B3. . .

Uchino fails to disclose or suggest the feature of "the at least two data buses are connected between the timing controller and the respective source drivers," as is set forth in instant claims 1 and 11 of the invention.

Uchino also fails to disclose or suggest a technology that reduces electric consumption by separate data sampling by the source driver of data separately output by the timing controller (see claims 17 and 18).

The Examiner admits to many of the failings of Uchino. At page 2 of the Office Action, the Examiner admits that "Uchino fails to specifically teach that the clock signals are input to the source drivers from a timing controller. . ." The Examiner also admits to further failures of Uchino, stating: "Uchino also fails to specifically teach the usage of two data buses transmitting data from the external device to the drivers." The Examiner further admits that "With reference

to claims 11 and 16, Uchino also fails to teach that the data synchronized with the respective clock signal for each odd/even numbered or R/G/B/ data through different data busses."

The invention, in contrast, shows a fundamentally different driving logic than that of Uchino. As shown in Figure 4 of the invention, the timing controller 47 feeds both clock signals CLK1, CLK2 and RGB data to source drivers 43 through at least two data buses DB1 and DB2. The timing controller 47 therefore provides the logic comparable to what the logical circuits 70a, 70b, 70c . . . of Uchino provide, but using a fundamentally different data bus configuration at a fundamentally different location in the circuit.

That is, by failing to disclose or suggest the limitation "the at least two data buses are connected between the timing controller and the respective source drivers," the applied art fails to fairly disclose or suggest each and every element of claims 1 and 11. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Further, while the invention pertains to separate sampling, Uchino teaches phase adjustment to promote simultaneous sampling. In describing the problem to be solved, Uchino at column 2 lines 39-43 states: "Therefore, the sampling is performed with a time lag from the original time at which the sampling must be originally performed, resulting in reduction of resolution and occurrence of ghost images. Accordingly, it is necessary to suppress the dispersion of phase among the sampling pulses." Uchino at column 7, lines 27-34 then describes the suppression of secondary sampling pulses to improve resolution. As a result, Uchino teaches away from the separate sampling of the invention. It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)

The Examiner then turns to Fig. 1 of Nakano and tries to graft the timing controller 100, clock signal and a single data bus 134 from a fundamentally different circuit logic onto that of Uchino. Although Nakano teaches a technology for lowering clock frequency, Nakano fails to disclose or suggest using at least two data buses and separate sampling to reduce energy consumption.

In her response to arguments in paragraph 5 of the Office Action, the examiner asserts:

> Uchino teaches that the clock signals are provided from an external source and Nakano teaches that the signals are provided from an external source (computer) through an interface, which comprises a control circuit. Therefore a person having ordinary skill in the art could combine Uchino and Nakano to produce the invention as recited in the claims. Nakano teaches reducing the clock signal frequency in order to reduce electromagnetic interference wherein the

timing controller outputs two clock signals of different phases to the source drivers along with RGB data as explained above.

However, the present invention saves energy not by phase shift (as in Uchino and Nakano), but by separate outputting and sampling where "the timing controller separately outputting R/G/B data synchronized with each output signal to the source drivers" (claim 1, *see also* claim 11) and "wherein the source drivers separately sample the data to thereby reduce electricity consumption." (claims 17 and 18).

As a result, the combination of Uchino and Nakano fails to suggest the invention of claims 1 and 11 to one of ordinary skill sufficient to allege *prima facie* obviousness.

The Examiner then turns to Itakura for teachings pertaining to having the number of data busses in proportion to the number of clock signals. However, these teachings of Itakura fail to address the deficiencies of Uchino and Nakano in suggesting the invention. As a result, the combination of Uchino, Nakano and Itakura would fail to motivate one having ordinary skill in the art to produce the invention of claims 1 and 11. A *prima facie* case of obviousness has thus not been made. Claims depending on claims 1 and 11 are patentable for at least the above reasons.

These rejections are overcome and withdrawal thereof is respectfully requested.

Prior Art Cited But Not Utilized By The Examiner

The prior art cited but not utilized by the Examiner shows the status of the conventional art that the invention supercedes. No additional remarks are accordingly necessary.

Priority

The Examiner has acknowledged priority most recently in the Office Action Summary of the Office Action mailed March 22, 2004.

Conclusion

The Examiner's rejections have been overcome, obviated or rendered moot. No issues remain. The Examiner is accordingly respectfully requested to allow the application.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert E. Goozner (Reg. No. 42,593) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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